



**VIT**  
BANGALORE

**MAVEN**  
SILICON  
Centre of Excellence in VLSI

CELEBRATING 15 YEARS OF EXCELLENCE IN VLSI TRAINING

# RISC-V RTL Verification

Blended - Online

**5000+**

Global Alumni

**250+**

Hiring Partners



Industry-Standard  
Curriculum



Live Q&A Review  
Sessions



24/7 VPN  
Access



Certificate



## VIT BANGALORE

VIT was established to provide quality higher education on par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education consistently. VIT Bangalore is established in the tradition of the VIT institutions to offer innovative programmes and prepare the leaders of tomorrow. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence.

## MAVEN SILICON

Maven Silicon is a leading provider of VLSI training for students and professionals. We offer a range of high-quality VLSI training programs and internships, taught by experienced industry professionals, aimed at helping engineers to upskill and advance their careers in the fast-growing Semiconductor Industry. From digital design and verification to physical design and design for testing, Maven Silicon covers a wide variety of topics along with labs and projects through Industry standard EDA tools. Our state-of-the-art training facilities, coupled with innovative training methods, provide students with hands-on experience and a strong foundation in the latest VLSI technologies. Our curriculum is designed to meet the demands of the industry and is constantly updated to keep pace with the latest advancements. In addition, Maven Silicon offers flexible scheduling options and customized training programs to accommodate student's busy schedules.

With a commitment to excellence and a passion for empowering students and professionals, Maven Silicon is dedicated to providing the highest quality hands-on training to help engineers reach their full potential in the Semiconductor industry.

My vision is to create an excellent learning ecosystem of superior technical expertise, hands-on training experience, and industry-oriented courses with innovative learning processes.

For more than 15 years, Maven Silicon has been a benchmark for the VLSI training ecosystem in India, offering high-quality VLSI training courses for VLSI aspirants, professionals, and organizations across the globe.

**Sivakumar P R**  
Founder and CEO



Our CEO, Sivakumar P R, has 25+ years of experience in the engineering and semiconductor industries. He has worked as a Verification Consultant in the top EDA companies like Synopsys, Cadence, and Mentor Graphics. During this tenure, he worked very closely with various ASIC and FPGA design houses and helped them to use the EDA solutions effectively for the successful tape-outs of multi-million gate designs.

To know more about our CEO, visit <https://www.linkedin.com/in/sivapr/>

# Three reasons to muse with **MAVEN SILICON**

## 01 **Dynamic VLSI courses designed and delivered by Industry experts**

Maven Silicon is the Best VLSI training center which provides high-class industry standard VLSI training. The courses have been designed by industry experts, based on the job opportunities and career growth in the semiconductor industry and we keep updating our VLSI Curriculum as per the latest industry trends.

---

## 02 **Superior Training Methodology and Infrastructure**

Our training methodology is unique. It helps our students to learn even complex technologies in a short span of time and make them experts. 70% of the course time is dedicated to the labs, mini projects, and the final project. Our training courses help you to acquire the technical skills which are highly required to get a job in the semiconductor industry.

---

## 03 **Hands on Learning**

This program offers hands on experience with various verification methodologies such as Constraint Random Coverage Driven Verification (CRCDV), Assertion Based Verification (ABV) using the languages like SystemVerilog and Methodologies like UVM on the project life cycle from Verification planning to Verification signoff, making the trainees industry ready. And also, this program offers understanding on RISC-V ISA and hands on experience on Verification methodology for verifying the RISC-V based designs and achieve coverage closure.

## EDA Partner

The Siemens logo is displayed in white text on a dark teal rounded rectangular background.

Siemens is a leader in Electronic Design Automation. Its innovative products and solutions help engineers conquer design challenges in the seemingly daunting world of board and chip design.

<https://eda.sw.siemens.com/en-US/>

The Synopsys logo is displayed in white text on a dark teal rounded rectangular background.

Synopsys is at the forefront of Smart Everything with the world's most advanced tools for silicon chip design, verification, IP integration, and application.

<https://www.synopsys.com/>

## COURSE CURRICULUM

# RISC-V

## RTL Verification

37 Modules

OS - Linux Ubuntu | EDA Tools - Siemens - Questasim

### Introduction to Linux

## Module I

- Components of UNIX system
- Directory Structure
- Utilities and Commands
- Vi Editor

### Verilog – HDL

## Module II

- Introduction to Verilog HDL
- Setting Expectations - Course Agenda
- Data Types
- Verilog Operators
- Verilog for Verification
- Assignments
- Structured Procedures
- Synthesis Coding Style
- Finite State Machine
- Verilog Labs

### Advanced Verilog

## Module III

- Self checking Testbenches
- Named events and stratified event queue

### Code Coverage

## Module IV

- Statement coverage
- Branch Coverage
- Expression Coverage
- Path Coverage
- Toggle Coverage
- FSM - State, Transition coverage

### Advanced Verilog & Code Coverage Labs

### Design Automation using Scripts Perl

## Module V

- Introduction to Perl
- Functions and Statements
- Numbers, Strings, and Quotes
- Comments and Loops
- Regular Expressions
- File Operations

### PERL Labs

### Verification Methodology Overview

## Module VI

- Introduction to Verification Methodology
- Verification Process
- Reusable TB
- Verification Environment Architecture
- Constraint Random Coverage Driven Verification
- Verification Methodologies & Summary

### SystemVerilog Language Concepts

## Module VII

- SystemVerilog Concepts Agenda
- SystemVerilog Virtual Interface
- SystemVerilog Randomization & Functional Coverage
- SystemVerilog OOP
- SystemVerilog Overview
- SystemVerilog Transactions
- SystemVerilog TB Architecture

### SystemVerilog Datatypes

## Module VIII

- SystemVerilog Introduction & Logic Data Type
- 2 State, Struct & Enum
- Strings, Packages & Summary

### SystemVerilog Memories

## Module IX

- Introduction, Packed and Multi-Dimensional Arrays
- Dynamic Arrays & Queues
- Associative Arrays, Array Methods & Summary

### SystemVerilog Tasks & Functions

## Module X

- Introduction, Void Functions, Function return & Automatic Task
- Pass by value & ref and Summary

### SystemVerilog Interfaces

## Module XI

- Introduction, Verilog ports Vs SV Interface
- Modports & Clocking Block
- SV Interfaces - Examples & Summary

### SystemVerilog Object Oriented Programming – Basics

## Module XII

- Introduction, Class Data Type & Objects
- Constructor, Null Object, Object assignments and copy
- Shallow Vs Deep Copy & Summary

### SystemVerilog Object Oriented Programming – Advanced

## Module XIII

- Introduction, Inheritance & Super keyword
- Static properties & methods, Pass by reference
- Polymorphism, \$cast, Virtual & Parametrised classes, Summary

## COURSE CURRICULUM

# RISC-V

## RTL Verification

37 Modules

OS - Linux Ubuntu | EDA Tools - Siemens - Questasim

### SystemVerilog Randomization

## Module XIV

- Introduction, rand and randc
- Randomize, Pre and Post randomize methods & Constraints
- Set Membership & Summary

### SystemVerilog Virtual Interface

## Module XV

- Introduction, Implementation & Examples

### SystemVerilog Threads

## Module XVI

- Threads, Events, Mailbox and Semaphores

### SystemVerilog Functional Coverage

## Module XVII

- Introduction & CRCDV
- Covergroup, Coverpoint, Bins, Cross, Methods & Summary

### Case Study 1 : Dual port RAM – SV TB

### Case Study 2 : Maven SoC – SV TB

### SystemVerilog Labs

### SystemVerilog - Reference Book

### SystemVerilog Assertions

## Module XVIII

- Introduction and types of assertion
- SVA building blocks, system functions
- Writing sequences and implication operators
- Repetition operators and sequence composition
- Miscellaneous concepts and connecting assertions to DUT

### SystemVerilog Assertions Labs

### SVA Reference Book

### Pilot Project – SystemVerilog

## Module XIX

- Understanding the specification
- Developing Verification plan & TB Architecture,
- Defining Interface blocks
- Developing various Transactors – Drivers, Monitors, Reference Model
- Developing SB and Verifying various test scenarios
- Coverage closure with regression testing

### Universal Verification Methodology Overview

## Module XX

- Introduction to UVM
- UVM Concepts
- UVM SOC TB
- UVM AHB UVC
- UVM SOC TB Examples

### UVM TB Architecture and Base Class Hierarchy

## Module XXI

- UVM Testbench Architecture
- UVM Base Class Hierarchy

### UVM Factory

## Module XXII

- Importance of using factory
- Registration Process
- Create Method and Factory Overriding

### UVM – Stimulus Modelling & Testbench Overview

## Module XXIII

- Predefined Methods and Field Registration Process
- Overriding the predefined do \_ methods
- UVM – TB Overview

### UVM Phases & Reporting Mechanism

## Module XXIV

- UVM Phases – Necessity of Phases & pre-run Phases
- UVM Phases – Run Phase, post-run Phases and Objection Mechanism
- UVM Reporting Mechanism

### UVM TLM Ports and Configuration

## Module XXV

- UVM TLM Ports – Blocking put and get ports
- UVM TLM Ports – TLM FIFO and Analysis Ports
- UVM Configuration – Introduction to Configuration Facility
- UVM Configuration – Configuration class and Configuration of Virtual Interface



## COURSE CURRICULUM

# RISC-V

## RTL Verification

37 Modules

OS - Linux Ubuntu | EDA Tools - Siemens - Questasim

### UVM - Creating UVM Testbench Components

## Module XXVI

- Creating UVM TB Components - Sequencers & Drivers
- Creating UVM TB Components - Monitor, Agents, Env and Testcases

### UVM Sequences

## Module XXVII

- UVM Sequences - Introduction and Sequence item flow
- UVM Sequences - Starting the sequences and Default Sequence
- UVM Virtual Sequences & Virtual Sequencers - Introduction
- UVM Virtual Sequences & Virtual Sequencers - implementation

### UVM Callbacks & Events

## Module XXVIII

- UVM Callbacks
- UVM Events

### UVM - Creating Scoreboard

### UVM - Register Abstraction Layer

## Module XXX

- UVM RAL - Intro & Definition of Register Block
- UVM RAL - Adapter, Predictor and Integration
- UVM RAL - Definition of Register Sequences

### UVM Labs

### UVM Reference Book

### Pilot Project - UVM

## Module XXXI

- Understanding the specification
- Developing Verification plan & TB Architecture,
- Defining Interface blocks
- Development of Source agent , transaction class & sequence
- Development of Destination agent , transaction class & sequence
- Developing Scoreboard and cover groups
- Verifying various test scenarios
- Coverage closure with regression testing

### RISC V RV32I Processor

### RISC-V Instruction Set Architecture

## Module XXXIII

- RISC-V processor overview
- RISC-V ISA Overview
- RV32I - R and I Type Instruction
- RV32I - S and B Type Instructions
- RV32I - J and U Type Instructions
- RV32I - Assembly Programs

### RISC-V RV32I RTL Architecture Design

## Module XXXIV

- RISC-V Execution Stages and Flow
- RISC-V Register File and RV32I Instructions Format
- RV32I - R and I Type ALU Datapath
- RV32I - S Type ALU Datapath - Load and Store
- RV32I - B and U Type ALU Datapath
- RV32I - J Type ALU Datapath - JAL and JALR

### RISC-V RV32I 5 stage Pipelined RTL Design

## Module XXXV

- CPU Performance and RISC-V 5 Stage Pipeline Overview
- RISC-V 5 stage Pipeline - Data Hazards and Design Approach
- RISC-V 5 Stage Pipeline - Control Hazards and Design Approach

### RISC-V RV32I Processor Verification

## Module XXXVII

- Understanding the specification Under-standing the specification
- Developing Verification plan & TB Architecture
- Defining Interface blocks
- Developing reset agent, Instruction agent.
- Developing Data Agent
- Implementing RAL model
- Developing Reference model and Scoreboard and cover groups.
- Developing various test scenarios to verify all the types of instructions
- Coverage closure with regression testing

### Industry Standard Project



Centre of Excellence in VLSI

South Taluk, 21/1A, III Floor, MS Plaza,  
Gottigere Uttarahalli Hobli,  
Bannerghatta Main Rd, Bengaluru,  
Karnataka 560076

For More Details Contact VIT Bangalore

✉ [study@vitbangalore.in](mailto:study@vitbangalore.in) ☎ +91 6362906969

## Association & Partnerships



\*Logos are the trademarks of the respective organizations.