VIT BANGALORE

MAVEN SILICON
Centre of Excellence in VLSI

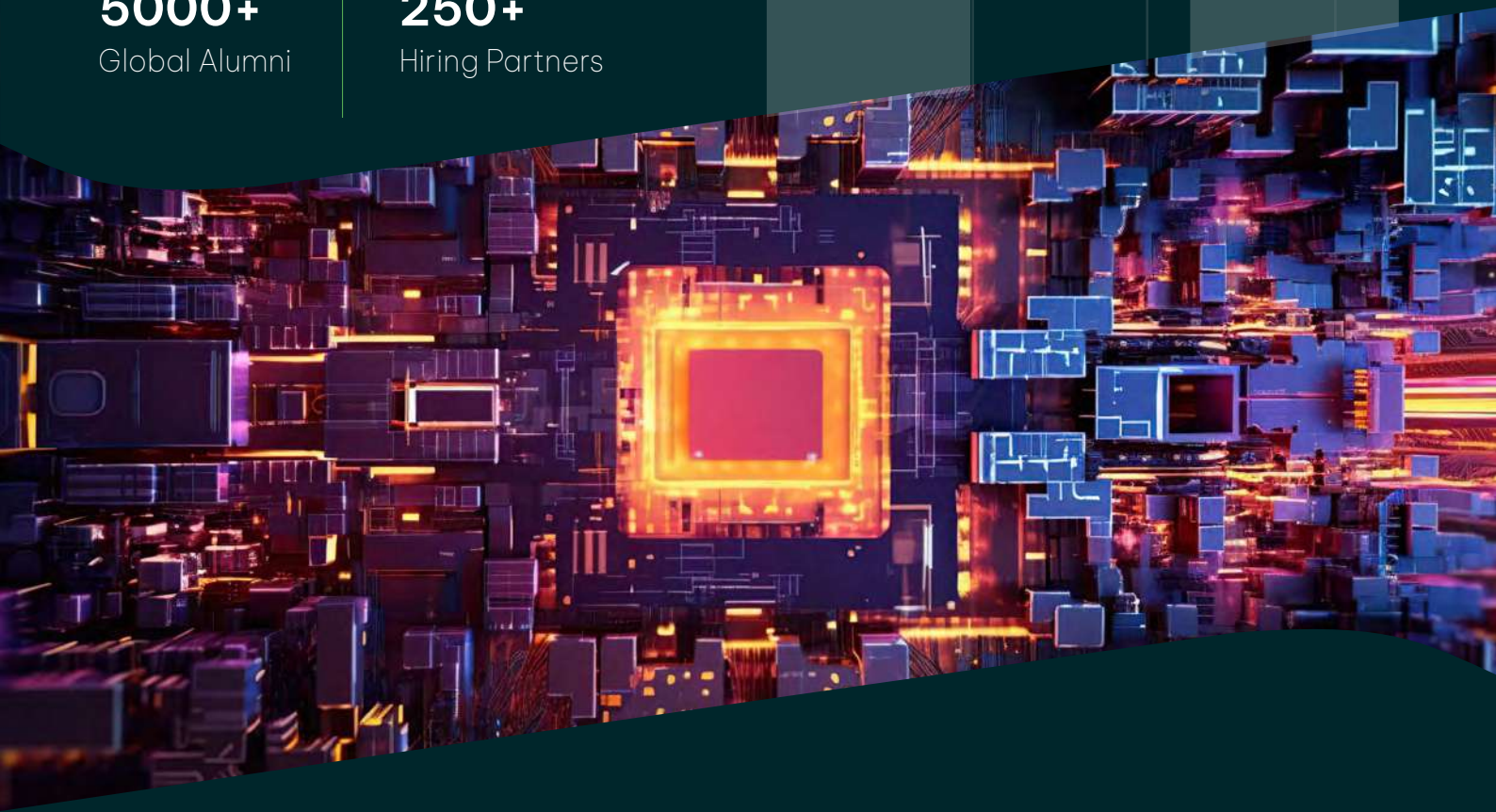
CELEBRATING 15 YEARS OF EXCELLENCE IN VLSI TRAINING

SystemVerilog Verification

Blended - Online

5000+
Global Alumni

250+
Hiring Partners



- Industry-Standard Curriculum
- Live Q&A Review Sessions
- 24/7 VPN Access
- Certificate

VIT BANGALORE

VIT was established to provide quality higher education on par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education consistently. VIT Bangalore is established in the tradition of the VIT institutions to offer innovative programmes and prepare the leaders of tomorrow. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence.

MAVEN SILICON

Maven Silicon is a leading provider of VLSI training for students and professionals. We offer a range of high-quality VLSI training programs and internships, taught by experienced industry professionals, aimed at helping engineers to upskill and advance their careers in the fast-growing Semiconductor Industry. From digital design and verification to physical design and design for testing, Maven Silicon covers a wide variety of topics along with labs and projects through Industry standard EDA tools. Our state-of-the-art training facilities, coupled with innovative training methods, provide students with hands-on experience and a strong foundation in the latest VLSI technologies. Our curriculum is designed to meet the demands of the industry and is constantly updated to keep pace with the latest advancements. In addition, Maven Silicon offers flexible scheduling options and customized training programs to accommodate student's busy schedules.

With a commitment to excellence and a passion for empowering students and professionals, Maven Silicon is dedicated to providing the highest quality hands-on training to help engineers reach their full potential in the Semiconductor industry.

My vision is to create an excellent learning ecosystem of superior technical expertise, hands-on training experience, and industry-oriented courses with innovative learning processes.

For more than 15 years, Maven Silicon has been a benchmark for the VLSI training ecosystem in India, offering high-quality VLSI training courses for VLSI aspirants, professionals, and organizations across the globe.

Sivakumar P R
Founder and CEO

Our CEO, Sivakumar P R, has 25+ years of experience in the engineering and semiconductor industries. He has worked as a Verification Consultant in the top EDA companies like Synopsys, Cadence, and Mentor Graphics. During this tenure, he worked very closely with various ASIC and FPGA design houses and helped them to use the EDA solutions effectively for the successful tape-outs of multi-million gate designs.

To know more about our CEO, visit https://www.linkedin.com/in/sivapr/

Three reasons to muse with MAVEN SILICON

01 Dynamic VLSI courses designed and delivered by Industry experts

Maven Silicon is the Best VLSI training center which provides high-class industry standard VLSI training. The courses have been designed by industry experts, based on the job opportunities and career growth in the semiconductor industry and we keep updating our VLSI Curriculum as per the latest industry trends.

02 Superior Training Methodology and Infrastructure

Our training methodology is unique. It helps our students to learn even complex technologies in a short span of time and make them experts. 70% of the course time is dedicated to the labs, mini projects, and the final project. Our training courses help you to acquire the technical skills which are highly required to get a job in the semiconductor industry.

03 Hands on Learning

This program offers hands on experience with various verification methodologies such as Constraint Random Coverage Driven Verification (CRCDV),using the languages like SystemVerilog on the project life cycle from Verification planning to Verification signoff, making the trainees industry ready.

EDA Partner

SIEMENS

Siemens is a leader in Electronic Design Automation. Its innovative products and solutions help engineers conquer design challenges in the seemingly daunting world of board and chip design.

https://eda.sw.siemens.com/en-US/

SYNOPSYS®

Synopsys is at the forefront of Smart Everything with the world's most advanced tools for silicon chip design, verification, IP integration, and application.

https://www.synopsys.com/

COURSE CURRICULUM

SystemVerilog Verification

14 Modules

OS - Linux Ubuntu | **EDA Tools -** Siemens - Questasim

Introduction to Linux

Module I

- Components of UNIX system
- Directory Structure
- Utilities and Commands
- Vi Editor

Verification Methodology Overview

Module II

- Introduction to Verification Methodology
- Verification Process
- Reusable TB
- Verification Environment Architecture
- Constraint Random Coverage Driven Verification
- Verification Methodologies & Summary

SystemVerilog Language Concepts

Module III

- SystemVerilog Concepts Agenda
- SystemVerilog Virtual Interface
- SystemVerilog Randomization & Functional Coverage
- SystemVerilog OOP
- SystemVerilog Overview
- SystemVerilog Interface
- SystemVerilog Transactions
- SystemVerilog TB Architecture

SystemVerilog Datatypes

Module IV

- SystemVerilog Introduction & Logic Data Type
- 2 State, Struct & Enum
- Strings, Packages & Summary

SystemVerilog Memories

Module V

- Introduction, Packed and Multi-Dimensional Arrays
- Dynamic Arrays & Queues
- Associative Arrays, Array Methods & Summary

SystemVerilog Tasks & Functions

Module VI

- Introduction, Void Functions, Function return & Automatic Task
- Pass by value & ref and Summary

SystemVerilog Interfaces

Module VII

- Introduction, Verilog ports Vs SV Interface
- Modports & Clocking Block
- SV Interfaces - Examples & Summary

SystemVerilog Object Oriented Programming – Basics

Module VIII

- Introduction, Class Data Type & Objects
- Constructor, Null Object, Object assignments and copy
- Shallow Vs Deep Copy & Summary

SystemVerilog Object Oriented Programming – Advanced

Module IX

- Introduction, Inheritance & Super keyword
- Static properties & methods, Pass by reference
- Polymorphism, $cast, Virtual & Parametrised classes, Summary

SystemVerilog Randomization

Module X

- Introduction, rand and randc
- Randomize, Pre and Post randomize methods & Constraints
- Set Membership & Summary

SystemVerilog Virtual Interface

Module XI

- Introduction, Implementation & Examples

SystemVerilog Threads

Module XII

- Threads, Events, Mailbox and Semaphores

SystemVerilog Functional Coverage

Module XIII

- Introduction & CRCDV
- Covergroup, Coverpoint, Bins, Cross, Methods & Summary

SystemVerilog Labs

SV Lab Setup guide - Reference Manuals

- SV Labs User Guide
- VPN Configuration Guide

SystemVerilog - Quick Reference Guide

Pilot Project

Module XIV

- Understanding the specification
- Developing Verification plan & TB Architecture,
- Defining Interface blocks
- Developing various Transactors - Drivers, Monitors, Reference Model
- Developing SB and Verifying various test scenarios
- Coverage closure with regression testing

MAVEN SILICON®

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South Taluk, 21/1A, III Floor, MS Plaza,
Gottigere Uttarahalli Hobli,
Bannerghatta Main Rd, Bengaluru,
Karnataka 560076

For More Details Contact VIT Bangalore

training@vitbangalore.ac.in +91 6362906969 https://vitbangalore.in/life/

Association & Partnerships

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