



**VIT**  
BANGALORE

**MAVER**  
SILICON  
Centre of Excellence in VLSI

CELEBRATING 15 YEARS OF EXCELLENCE IN VLSI TRAINING

# UVM Verification

Blended - Online

**5000+**

Global Alumni

**250+**

Hiring Partners



Industry-Standard  
Curriculum



Live Q&A Review  
Sessions



24/7 VPN  
Access



Certificate

## VIT BANGALORE

VIT was established to provide quality higher education on par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education consistently. VIT Bangalore is established in the tradition of the VIT institutions to offer innovative programmes and prepare the leaders of tomorrow. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence.

## MAVEN SILICON

Maven Silicon is a leading provider of VLSI training for students and professionals. We offer a range of high-quality VLSI training programs and internships, taught by experienced industry professionals, aimed at helping engineers to upskill and advance their careers in the fast-growing Semiconductor Industry. From digital design and verification to physical design and design for testing, Maven Silicon covers a wide variety of topics along with labs and projects through Industry standard EDA tools. Our state-of-the-art training facilities, coupled with innovative training methods, provide students with hands-on experience and a strong foundation in the latest VLSI technologies. Our curriculum is designed to meet the demands of the industry and is constantly updated to keep pace with the latest advancements. In addition, Maven Silicon offers flexible scheduling options and customized training programs to accommodate student's busy schedules.

With a commitment to excellence and a passion for empowering students and professionals, Maven Silicon is dedicated to providing the highest quality hands-on training to help engineers reach their full potential in the Semiconductor industry.

My vision is to create an excellent learning ecosystem of superior technical expertise, hands-on training experience, and industry-oriented courses with innovative learning processes.

For more than 15 years, Maven Silicon has been a benchmark for the VLSI training ecosystem in India, offering high-quality VLSI training courses for VLSI aspirants, professionals, and organizations across the globe.

**Sivakumar P R**  
Founder and CEO



Our CEO, Sivakumar P R, has 25+ years of experience in the engineering and semiconductor industries. He has worked as a Verification Consultant in the top EDA companies like Synopsys, Cadence, and Mentor Graphics. During this tenure, he worked very closely with various ASIC and FPGA design houses and helped them to use the EDA solutions effectively for the successful tape-outs of multi-million gate designs.

To know more about our CEO, visit <https://www.linkedin.com/in/sivapr/>

# Three reasons to muse with **MAVEN SILICON**

## 01 **Dynamic VLSI courses designed and delivered by Industry experts**

Maven Silicon is the Best VLSI training center which provides high-class industry standard VLSI training. The courses have been designed by industry experts, based on the job opportunities and career growth in the semiconductor industry and we keep updating our VLSI Curriculum as per the latest industry trends.

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## 02 **Superior Training Methodology and Infrastructure**

Our training methodology is unique. It helps our students to learn even complex technologies in a short span of time and make them experts. 70% of the course time is dedicated to the labs, mini projects, and the final project. Our training courses help you to acquire the technical skills which are highly required to get a job in the semiconductor industry.

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## 03 **Hands on Learning**

This program offers hands-on experience with industry-standard verification methodology which is UVM, on the verification project life cycle which involves processes like Verification planning, TB development, developing regression Test Suite, and Verification signoff, making the trainees industry-ready.

## EDA Partner

**SIEMENS**

Siemens is a leader in Electronic Design Automation. Its innovative products and solutions help engineers conquer design challenges in the seemingly daunting world of board and chip design.

<https://eda.sw.siemens.com/en-US/>

**SYNOPSYS®**

Synopsys is at the forefront of Smart Everything with the world's most advanced tools for silicon chip design, verification, IP integration, and application.

<https://www.synopsys.com/>

## COURSE CURRICULUM

# UVM Verification

13 Modules

OS - Linux Ubuntu | EDA Tools - Siemens - Questasim

## Verification Methodology Overview

### Module I

- Introduction to Verification Methodology
- Verification Process
- Reusable TB
- Verification Environment Architecture
- Constraint Random Coverage Driven Verification
- Verification Methodologies & Summary

## Universal Verification Methodology Overview

### Module II

- Introduction to UVM
- UVM Concepts
- UVM SoC TB
- UVM AHB UVC
- UVM SOC TB Examples

## UVM TB Architecture and Base Class Hierarchy

### Module III

- UVM Testbench Architecture
- UVM Base Class Hierarchy

## UVM Factory

### Module IV

- Importance of using factory
- Registration Process
- Create Method and Factory Overriding

## UVM - Stimulus Modelling & Testbench Overview

### Module V

- Predefined Methods and Field Registration Process
- Overriding the predefined do \_ methods
- UVM - TB Overview

## UVM Phases & Reporting Mechanism

### Module VI

- UVM Phases - Necessity of Phases & pre-run Phases
- UVM Phases - Run Phase, post-run Phases and Objection Mechanism
- UVM Reporting Mechanism

## UVM TLM Ports and Configuration

### Module VII

- UVM TLM Ports - Blocking put and get ports
- UVM TLM Ports - TLM FIFO and Analysis Ports
- UVM Configuration - Introduction to Configuration Facility
- UVM Configuration - Configuration class and Configuration of Virtual Interface

## UVM - Creating UVM Testbench Components

### Module VIII

- Creating UVM TB Components - Sequencers & Drivers
- Creating UVM TB Components - Monitor, Agents, Env and Testcases

## UVM Sequences

### Module IX

- UVM Sequences - Introduction and Sequence item flow
- UVM Sequences - Starting the sequences and Default Sequence
- UVM Virtual Sequences & Virtual Sequencers - Introduction
- UVM Virtual Sequences & Virtual Sequencers - implementation

## UVM Callbacks & Events

### Module X

- UVM Callbacks
- UVM Events

## UVM - Creating Scoreboard

## UVM - Register Abstraction Layer

### Module XII

- UVM RAL - Intro & Definition of Register Block
- UVM RAL - Adapter, Predictor and Integration
- UVM RAL - Definition of Register Sequences

## UVM Labs

## UVM Reference Book

## Pilot Project

### Module XIII

- Understanding the specification
- Developing Verification plan & TB Architecture,
- Defining Interface blocks
- Development of Source agent , transaction class & sequence
- Development of Destination agent , transaction class & sequence
- Developing Scoreboard and cover groups
- Verifying various test scenarios
- Coverage closure with regression testing



Centre of Excellence in VLSI

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## Association & Partnerships



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